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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/686,072
Filing Date: October 11, 2000
Appellant(s): WELLAND ET AL.

Bruce A Johnson
For Appellant

SUPPLEMENT EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/03/2005 and the Responses filed 11/20/06 and 3/22/06 appealing from the Office Action mailed 7/12/2004.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,111,470	Dufour	8-2000
6,087,865	Bradley	7-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 3-4 and 52-54 and 66-79 and 81-85 are rejected under 35 USC 103 (a) as being unpatentable Bradley (US 6,087,865) in view of Dufour (US 6,111,470).

Bradley discloses in Figure 5 a PLL circuit (203) comprising:

- a first fixed-value non programmable divider (221) for receiving an input signal (198) and dividing the input signal by a first fixed amount Q;
- a second fixed-value non programmable divider (220) for receiving the divided signal from the first fixed value diver (221) and further dividing the input signal by a second fixed amount R;
- a phase detector (213); and
- a VCO circuitry (210).
- Wherein the interference noise inherently is reduced at an output of the VCO circuitry by the arrangement of the dividers (221,220).

However, Bradley does not disclose that the PLL circuit is implemented on an integrated circuit, one of the divider divides the input frequency by the first fixed value of thirteen and

other divider divides by the second fixed value of five as recited in claims 3 and 68, and the product of the first and second fixed values is sixty-five as recited in claims 67 and 78.

Nevertheless, Dufour teaches in Figure 1 a PLL circuit implemented on an integrated circuit for reducing size.

It would have been obvious to a person having skill in the art at the time the invention was made to implement the PLL circuit of Bradley on an integrated circuit taught by Dufour for the purpose of reducing size.

Although Bradley does not specify that one of the dividers (221, 220) divides the input frequency by thirteen (Q=13) and the other of the dividers divides the input frequency by five (R=5) or the product of the first and second fixed value (QxR) is sixty-five; however, Bradley suggests on lines 1-27, column 7, that the synthesizer is built to have an output frequency by selecting the dividers (220-222) having the division factors (Q, R, M) based on the formula Fs=FIN(M/(Q*R)). For example, the output frequency range of the synthesizer would be 240-300MHZ when the factor N is equal to 4 based on Table A in column 6. Thus, selecting the dividers having optimum fixed values Q and R of Bradley for providing a predetermined output frequency is considered to be a matter of design expedient for an engineer depending upon a particular application in which the circuit of Bradley is to be used.. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). It would have been obvious to a person having the skill in the art at the time the invention was made to select the fixed values of the dividers of Bradley as claimed for the purpose of providing a predetermined frequency synthesizer output.

(10) Response to Argument

The Appellant argues in the second paragraph of page 12 of the Appeal Brief that there is no motivation to combine the Bradley reference with the Dufour reference. The argument is not persuasive. Bradley discloses in Figure 5 a phase lock loop circuit (203) comprising a phase detector (213), the VCO circuitry (210) and the dividers (221, 220) but does not disclose that the PLL circuit is implemented on an integrated circuit. Dufour suggests in Figure 1 to implement a PLL circuit on an integrated circuit since the integrated circuit is a small unit or a package which is made as a chip for reducing the circuit size. Thus, the integrated circuit suggested by Dufour can be applied in the circuit Bradley. One skilled in the art would have been motivated to implement the PLL circuit of Bradley on an integrated circuit as suggested by Dufour in order to reduce the size of the PLL circuit.

The Appellant argues in the last paragraph of pages 13, in the second paragraph of page 14, in the second and fourth paragraphs of page 15 and in the last paragraph of page 16 of the Brief that the division factors (Q, R) of the dividers (220, 221) of Bradley are not fixed and are designed to be interchangeable as desired because the dividers (220, 221) are programmable dividers so that Bradley does not suggest the use of fixed-value dividers or fixed non-programmable division factors as claimed. The arguments are not persuasive by the following reasons:

- Firstly, Figures 4-5 of Bradley shows that the dividers (220, 221) are not the programmable dividers or variable dividers because they do not have any control signal or a programming control signal for adjusting or programming the division factors (R, Q). Thus, the dividers (220, 221) are fixed dividers.

- Secondly, the circuit as shown in Figure 5 of Bradley is the designed circuit diagram

of the synthesizer. The dividers (220, 221, 222) are the fixed components and theirs division factors (Q, R, M) are not specified but they are allowed to be selected to provide desired output frequency signals for the synthesizer accordance with the formula Fs=FIN(M/(Q*R)), see column 7. The selected division factors (Q, R, M) would be fixed after selection. Moreover, the synthesizer circuit of Bradley has the same structure as the structure of the circuit being shown in Figure 26 of the present invention in which the division factors (R1, R2) of the dividers (2604, 2605) are selected as a number 15 and a number 5 as recited in claim 3 or the product of the first and second division factors is equal to 65 as recited in claim 67. Thus, the claimed first and second fixed value dividers as recited in claim 1 are anticipated by the dividers (220, 221) of Bradley.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is 571-272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent (Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Dinh Le
Primary Examiner

Conferees:

Timothy Callahan

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22 March 2007